

## WEST Search History

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DATE: Monday, April 12, 2004

| <u>Hide?</u>             | <u>Set</u> | <u>Query</u>   | <u>Hit Count</u> |
|--------------------------|------------|--|------------------|
|                          |            | <i>DB=PGPB,USPT,JPAB; PLUR=YES; OP=OR</i>                                  |                  |
| <input type="checkbox"/> | L56        | L53 and (hdl or vhdl)  | 1                |
| <input type="checkbox"/> | L55        | L53 and (hdl or vhdl) and (synthes\$ or design\$)                          | 1                |
| <input type="checkbox"/> | L54        | L53 and (hdl or vhdl) and simula\$ and (synthes\$ or design\$)             | 1                |
| <input type="checkbox"/> | L53        | l1 and L52   | 56               |
| <input type="checkbox"/> | L52        | compatib\$ same compil\$   | 1732             |
| <input type="checkbox"/> | L51        | L50 and l1   | 3                |
| <input type="checkbox"/> | L50        | compatib\$ same compil\$ same (hardware or technolod\$)                    | 234              |
| <input type="checkbox"/> | L49        | hdl same compil\$ same dependen\$ same (hardware or technolog\$)           | 12               |
| <input type="checkbox"/> | L48        | L47 and (hdl or vhdl) and synthes\$ and simulat\$                          | 6                |
| <input type="checkbox"/> | L47        | L46 and l1 and l14   | 174              |
| <input type="checkbox"/> | L46        | compil\$ same code same generat\$  | 8506             |
| <input type="checkbox"/> | L45        | L41 and (hdl or vhdl)  | 0                |
| <input type="checkbox"/> | L44        | L43 and (hdl or vhdl)  | 0                |
| <input type="checkbox"/> | L43        | L41 and relation\$ and (simula\$ or synthes\$ or design\$)                 | 35               |
| <input type="checkbox"/> | L42        | L41 and synthes\$ and simulat\$ and (hdl or vhdl or verilog or programm\$) | 2                |
| <input type="checkbox"/> | L41        | L40 and l1 and l14   | 44               |
| <input type="checkbox"/> | L40        | compil\$ same intermedia\$ same code                                       | 1662             |
| <input type="checkbox"/> | L39        | l1 and l27   | 5                |
| <input type="checkbox"/> | L38        | L37 and l1   | 2                |
| <input type="checkbox"/> | L37        | L36 and port and buffer and (flip adj flop)                                | 23               |
| <input type="checkbox"/> | L36        | L33 and compil\$ and ((high or low) same programming)                      | 31               |
| <input type="checkbox"/> | L35        | L33 and compil\$ and (high same low same programming)                      | 3                |
| <input type="checkbox"/> | L34        | L33 not l30  | 21               |
| <input type="checkbox"/> | L33        | L32 and programming and (code same (generat\$ or transform\$))             | 61               |
| <input type="checkbox"/> | L32        | L17 and (dependen\$ same (architecture or hardware or technolog\$))        | 87               |
| <input type="checkbox"/> | L31        | L28 not l30  | 12               |
| <input type="checkbox"/> | L30        | L29 and port and construct\$   | 40               |
| <input type="checkbox"/> | L29        | L28 and (code same (generat\$ or transform\$))                             | 41               |
| <input type="checkbox"/> | L28        | L27 and compil\$ and pars\$  | 52               |
| <input type="checkbox"/> | L27        | l17 and L26  | 62               |

## Search History Transcript

|                          |     |   |        |
|--------------------------|-----|---|--------|
| <input type="checkbox"/> | L26 | hardware same dependen\$  | 8965   |
| <input type="checkbox"/> | L25 | L24 and (flip adj flop)   | 16     |
| <input type="checkbox"/> | L24 | L23 and pars\$  | 23     |
| <input type="checkbox"/> | L23 | L22 and (code same (generat\$ or transform\$))  | 29     |
| <input type="checkbox"/> | L22 | L21 and construct   | 31     |
| <input type="checkbox"/> | L21 | L20 and port and (component or element or object)                                     | 40     |
| <input type="checkbox"/> | L20 | L19 and programming   | 43     |
| <input type="checkbox"/> | L19 | L18 and programmable  | 61     |
| <input type="checkbox"/> | L18 | L17 and compil\$ and intermedia\$   | 105    |
| <input type="checkbox"/> | L17 | L15 and (hdl or vhdl) and simulat\$ and synthes\$                                     | 162    |
| <input type="checkbox"/> | L16 | L15 and (hdl or vhdl) and simulat\$ or synthes\$                                      | 442717 |
| <input type="checkbox"/> | L15 | L14 and l12   | 994    |
| <input type="checkbox"/> | L14 | boolean same (logic or function or equation or expression)                            | 10787  |
| <input type="checkbox"/> | L13 | l7 and L12  | 157    |
| <input type="checkbox"/> | L12 | (target\$ or retarget\$) same (architecture or hardware or technolog\$)               | 38205  |
| <input type="checkbox"/> | L11 | L8 and (boolean same (equation or expression or function))                            | 156    |
| <input type="checkbox"/> | L10 | L8 and (reusea\$ or useable)  | 11     |
| <input type="checkbox"/> | L9  | L8 and (reusa\$ or useable)   | 28     |
| <input type="checkbox"/> | L8  | L7 and (target\$ or retarget\$)   | 196    |
| <input type="checkbox"/> | L7  | boolean and (vhdl or hdl) and synthes\$ and simulat\$ and (architecture or technolog) | 262    |
| <input type="checkbox"/> | L6  | L5 and cpla   | 0      |
| <input type="checkbox"/> | L5  | L4 and compil\$ and (target\$ or retarget\$)  | 10     |
| <input type="checkbox"/> | L4  | L1 and hdl and simulat\$  | 17     |
| <input type="checkbox"/> | L3  | L2 and (target\$ or retarget\$)   | 10     |
| <input type="checkbox"/> | L2  | L1 and hdl and synthes\$ and simulat\$  | 13     |
| <input type="checkbox"/> | L1  | boolean same object   | 2605   |

END OF SEARCH HISTORY

## Hit List

|                               |                                     |                       |                          |                           |
|-------------------------------|-------------------------------------|-----------------------|--------------------------|---------------------------|
| <a href="#">Clear</a>         | <a href="#">Generate Collection</a> | <a href="#">Print</a> | <a href="#">Fwd Refs</a> | <a href="#">Bkwd Refs</a> |
| <a href="#">Generate OACS</a> |                                     |                       |                          |                           |

Search Results - Record(s) 1 through 2 of 2 returned.

1. Document ID: US 20030216901 A1

Using default format because multiple data bases are involved.

L38: Entry 1 of 2

File: PGPB

Nov 20, 2003

PGPUB-DOCUMENT-NUMBER: 20030216901

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030216901 A1

TITLE: Design apparatus and a method for generating an implementable description of a digital system

PUBLICATION-DATE: November 20, 2003

INVENTOR-INFORMATION:

| NAME               | CITY       | STATE | COUNTRY | RULE-47 |
|--------------------|------------|-------|---------|---------|
| Schaumont, Patrick | Wijgmaal   |       | BE      |         |
| Vernalde, Serge    | Heverlee   |       | BE      |         |
| Cockx, Johan       | Pellenberg |       | BE      |         |

US-CL-CURRENT: 703/13

|                      |                       |                          |                       |                        |                                |                      |                           |                           |                             |                        |                      |                         |
|----------------------|-----------------------|--------------------------|-----------------------|------------------------|--------------------------------|----------------------|---------------------------|---------------------------|-----------------------------|------------------------|----------------------|-------------------------|
| <a href="#">Full</a> | <a href="#">Title</a> | <a href="#">Citation</a> | <a href="#">Front</a> | <a href="#">Review</a> | <a href="#">Classification</a> | <a href="#">Date</a> | <a href="#">Reference</a> | <a href="#">Sequences</a> | <a href="#">Attachments</a> | <a href="#">Claims</a> | <a href="#">KWMC</a> | <a href="#">Drawn D</a> |
|----------------------|-----------------------|--------------------------|-----------------------|------------------------|--------------------------------|----------------------|---------------------------|---------------------------|-----------------------------|------------------------|----------------------|-------------------------|

2. Document ID: US 6606588 B1

L38: Entry 2 of 2

File: USPT

Aug 12, 2003

US-PAT-NO: 6606588

DOCUMENT-IDENTIFIER: US 6606588 B1

TITLE: Design apparatus and a method for generating an implementable description of a digital system

|                      |                       |                          |                       |                        |                                |                      |                           |                           |                             |                        |                      |                         |
|----------------------|-----------------------|--------------------------|-----------------------|------------------------|--------------------------------|----------------------|---------------------------|---------------------------|-----------------------------|------------------------|----------------------|-------------------------|
| <a href="#">Full</a> | <a href="#">Title</a> | <a href="#">Citation</a> | <a href="#">Front</a> | <a href="#">Review</a> | <a href="#">Classification</a> | <a href="#">Date</a> | <a href="#">Reference</a> | <a href="#">Sequences</a> | <a href="#">Attachments</a> | <a href="#">Claims</a> | <a href="#">KWMC</a> | <a href="#">Drawn D</a> |
|----------------------|-----------------------|--------------------------|-----------------------|------------------------|--------------------------------|----------------------|---------------------------|---------------------------|-----------------------------|------------------------|----------------------|-------------------------|

|                       |                                     |                       |                          |                           |                               |
|-----------------------|-------------------------------------|-----------------------|--------------------------|---------------------------|-------------------------------|
| <a href="#">Clear</a> | <a href="#">Generate Collection</a> | <a href="#">Print</a> | <a href="#">Fwd Refs</a> | <a href="#">Bkwd Refs</a> | <a href="#">Generate OACS</a> |
|-----------------------|-------------------------------------|-----------------------|--------------------------|---------------------------|-------------------------------|

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|-------|-----------|
| Terms | Documents |
|-------|-----------|

## Hit List

|                      |                            |              |                 |                  |
|----------------------|----------------------------|--------------|-----------------|------------------|
| <b>Clear</b>         | <b>Generate Collection</b> | <b>Print</b> | <b>Fwd Refs</b> | <b>Bkwd Refs</b> |
| <b>Generate OACS</b> |                            |              |                 |                  |

Search Results - Record(s) 1 through 6 of 6 returned.

1. Document ID: US 20030216901 A1

Using default format because multiple data bases are involved.

L48: Entry 1 of 6

File: PGPB

Nov 20, 2003

PGPUB-DOCUMENT-NUMBER: 20030216901

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030216901 A1

TITLE: Design apparatus and a method for generating an implementable description of a digital system

PUBLICATION-DATE: November 20, 2003

INVENTOR-INFORMATION:

| NAME               | CITY       | STATE | COUNTRY | RULE-47 |
|--------------------|------------|-------|---------|---------|
| Schaumont, Patrick | Wijgmaal   |       | BE      |         |
| Vernalde, Serge    | Heverlee   |       | BE      |         |
| Cockx, Johan       | Pellenberg |       | BE      |         |

US-CL-CURRENT: 703/13

|      |       |          |       |        |                |      |           |           |             |        |      |          |
|------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|------|----------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KMPC | Drawn Ds |
|------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|------|----------|

2. Document ID: US 20020080174 A1

L48: Entry 2 of 6

File: PGPB

Jun 27, 2002

PGPUB-DOCUMENT-NUMBER: 20020080174

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020080174 A1

TITLE: System and method for configuring an instrument to perform measurement functions utilizing conversion of graphical programs into hardware implementations

PUBLICATION-DATE: June 27, 2002

INVENTOR-INFORMATION:

| NAME                | CITY   | STATE | COUNTRY | RULE-47 |
|---------------------|--------|-------|---------|---------|
| Kodosky, Jeffrey L. | Austin | TX    | US      |         |
| Andrade, Hugo       | Austin | TX    | US      |         |

## Record List Display

|                   |            |    |    |
|-------------------|------------|----|----|
| Odom, Brian Keith | Georgetown | TX | US |
| Butler, Cary Paul | Austin     | TX | US |
| Schultz, Kevin L. | Georgetown | TX | US |

US-CL-CURRENT: 345/762

|      |       |          |       |        |                |      |           |           |             |        |      |         |
|------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|------|---------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KM/C | Drawn D |
|------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|------|---------|

 3. Document ID: US 6608638 B1

L48: Entry 3 of 6

File: USPT

Aug 19, 2003

US-PAT-NO: 6608638

DOCUMENT-IDENTIFIER: US 6608638 B1

TITLE: System and method for configuring a programmable hardware instrument to perform measurement functions utilizing estimation of the hardware implementation and management of hardware resources

|      |       |          |       |        |                |      |           |           |             |        |      |         |
|------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|------|---------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KM/C | Drawn D |
|------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|------|---------|

 4. Document ID: US 6606588 B1

L48: Entry 4 of 6

File: USPT

Aug 12, 2003

US-PAT-NO: 6606588

DOCUMENT-IDENTIFIER: US 6606588 B1

TITLE: Design apparatus and a method for generating an implementable description of a digital system

|      |       |          |       |        |                |      |           |           |             |        |      |         |
|------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|------|---------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KM/C | Drawn D |
|------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|------|---------|

 5. Document ID: US 6584601 B1

L48: Entry 5 of 6

File: USPT

Jun 24, 2003

US-PAT-NO: 6584601

DOCUMENT-IDENTIFIER: US 6584601 B1

TITLE: System and method for converting graphical programs into hardware implementations which utilize probe insertion

|      |       |          |       |        |                |      |           |           |             |        |      |         |
|------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|------|---------|
| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KM/C | Drawn D |
|------|-------|----------|-------|--------|----------------|------|-----------|-----------|-------------|--------|------|---------|

 6. Document ID: US 6457164 B1

L48: Entry 6 of 6

File: USPT

Sep 24, 2002

## Record List Display

US-PAT-NO: 6457164

DOCUMENT-IDENTIFIER: US 6457164 B1

TITLE: Heterogeneous method for determining module placement in FPGAs

[Full](#) [Title](#) [Citation](#) [Front](#) [Review](#) [Classification](#) [Date](#) [Reference](#) [Sequences](#) [Attachments](#) [Claims](#) [KMC](#) [Drawn D.](#)[Clear](#)[Generate Collection](#)[Print](#)[Fwd Refs](#)[Bkwd Refs](#)[Generate OACS](#)

Terms

Documents

L47 and (hdl or vhdl) and synthes\$ and simulat\$

6

Display Format: [Change Format](#)[Previous Page](#)[Next Page](#)[Go to Doc#](#)